EE/CprE/SE 491 WEEKLY REPORT 3

Date: ***Feb 13th, 2023 – February 19th, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

For the third week, we learned more about the analog process flow and how it ties into the Efabless program. There are still some lingering questions about how everything comes together as a whole, but we have the building blocks of how the process should work. We made further progress on getting the Caravel analog framework working; however, some issues still remain. We are communicating with others in a Slack channel who will hopefully provide us with some help. Finally, we began to use and test some of the tools that will be used for this project.

Past week accomplishments

- Joshua Thater
    - Researched the analog process flow and how it ties into the Efabless process.
    - Figured out how the Caravel harness works for analog projects.
    - Designed rough steps of how the bring-up of an analog/mixed-signal design gets submitted to Efabless for tape-out.
- Aiden Petersen
    - Troubleshooted setting up Analog caravel framework
    - Researched how digital design works in a analog context.
- Matt Ottersen

    - Researched and tested analog simulation using xschem and ngspice
- Regassa Dukele
    - Researched analog design flow.
    - Designed analog circuit examples in XSCHEM and verified the simulation result.

Pending issues

- Caraval analog framework is still broken. Working within the Slack channel to see how to fix it.
- Questions remain about the Caravel harness chip and how it interacts with design.
- What does the netlist of an analog project look like, and how it can be hooked up to the Caravel harness.

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Reseached the analog process flow and wrote out rough steps of how it works.	5	20
Aiden Petersen	Troubleshot analog framework	10	21
Matt Ottersen	Researched analog simulation	5	15
Regassa Dukele	Researched analog design flow	6	16.5

Plans for the upcoming week

- Joshua Thater
    - Answer lingering questions on the Caravel harness chip.
    - Try to obtain a netlist of an analog project.
    - Figure out how the netlist can be used in the .gds file to work with the harness.
- Aiden Petersen
    - Finish setting up analog framework hopefully
    - Assist in creating a design process flowchart for advisor meeting
- Matt Ottersen
    - Further research analog simulation
    - Research digital and mixed signal simulation with xschem and ngspice
- Regassa Dukele
    - Researched analog design flow and worked on understanding how it fits into the design process.